THE 8255A PROGRAMMABLE PERIPHERAL INTERFACE

The 8255A is a widely used, programmable, parallel I/O device. It can be programmed to transfer data under various conditions, from simple I/O to interrupt I/O. It is flexible, versatile, and economical (when multiple I/O ports are required), but somewhat complex. It is an important general-purpose I/O device that can be used with almost any microprocessor.

The 8255A has 24 I/O pins that can be grouped primarily in two 8-bit parallel ports:
A and B, with the remaining eight bits as port C. The eight bits of port C can be used as individual bits or be grouped in two 4-bit ports: C_{UPPER} (C_U) and C_{LOWER}, (C_L), as in Figure 4.1(a). The functions of these ports are defined by writing a control word in the control register.

Figure 4.1(b) shows all the functions of the 8255A, classified according to two modes: the Bit Set/Reset (BSR) mode and the I/O mode. The BSR mode is used to set or reset the bits in port C. The I/O mode is further divided into three modes: Mode 0. Mode 1, and Mode 2. In Mode 0, all ports function as simple I/O ports. Mode 1 is a handshake mode whereby ports A and/or B use bits from port C as handshake signals. In the handshake mode, two type of I/O data transfer can be implemented: status check and interrupt. In Mode 2, port A can be set up for bidirectional data transfer using handshake signals from port C, and port B can be set up either in Mode 0 or Mode 1.

4.1.1 Block Diagram of the 8255A

The block diagram in Figure 4.2(a), shows two 8-bit ports (A and B), two 4-bit ports (C_U and C_L), the data bus buffer, and control logic. Figure 4.2(b) shows a simplified but expanded version of the internal structure, including a control register. This block diagram includes all the elements of a programmable device; port C performs functions similar to that of the status register in addition to providing handshake signals.

CONTROL LOGIC

The control section has six lines. Their functions and connections are as follows:

- RD (Read): This control signal enables the Read operation. When the signal is low, the MPU reads data from a selected I/O port of the 8255A.
- WR (Write): This control signal enables the Write operation. When the signal goes low, the MPU writes into a selected I/O port or the control register.
- RESET (Reset): This is an active high signal; it clears the control register and sets all ports in the input mode.
- CS, A0, and A1: These are device select signals. CS is connected to a decoded address, and A0 and A1 are generally connected to MPU address lines A0 and A1, respectively.

The CS signal is the master Chip Select, and A0 and A1 specify one of the I/O ports or the control register as given below:

$\overline{CS}$	A_1	A_0	Selected
0	0	0	Port A
0	0	1	Port B
0	1	0	Port C
0	1	1	Control Register
1	X	X	8255A is not selected.

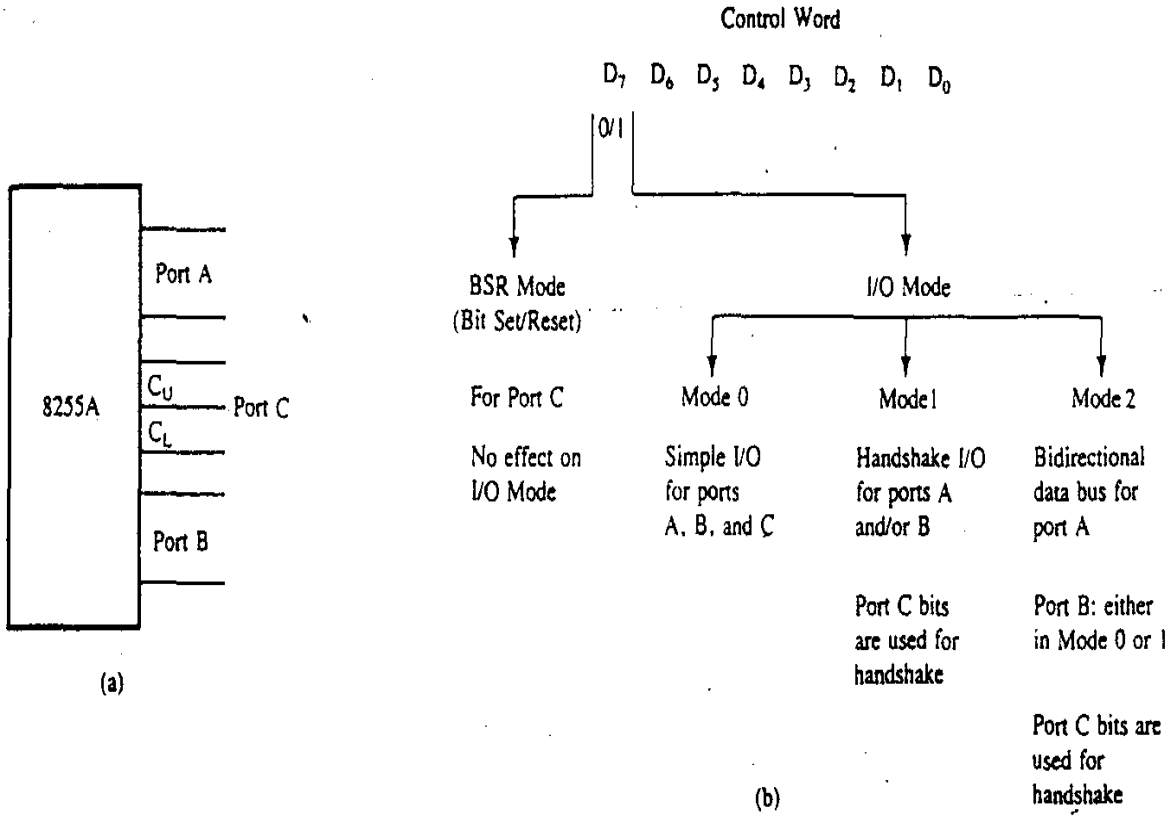
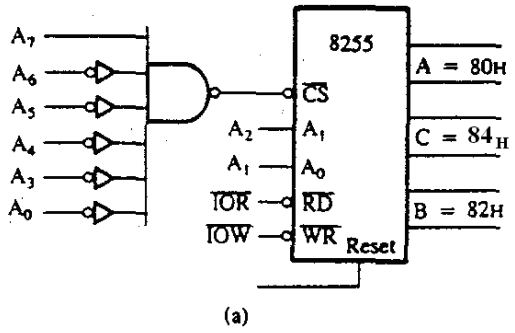


FIGURE 4.1: 8255A 1/0 Ports (a) and Their Modes (b)

As an example, the port addresses in Figure 4.3(a) are determined by the CS, A0, and A1 lines. The CS line goes low when A7 = 1 and A6 through A3 are at logic 0, and A0 is at logic 0. When these signals are combined with A2 and A1, the port addresses take the even addresses range from 80H to 86H, as shown in Figure 4.3(b).



$\overline{CS}$								Hex Address	Port
A7	A6	A5	A4	A3	A0	A2	A1		
1	0	0	0	0	0	0	0	= 80H	A
						0	1	= 82H	B
						1	0	= 84H	C
						1	1	= 86H	Control Register

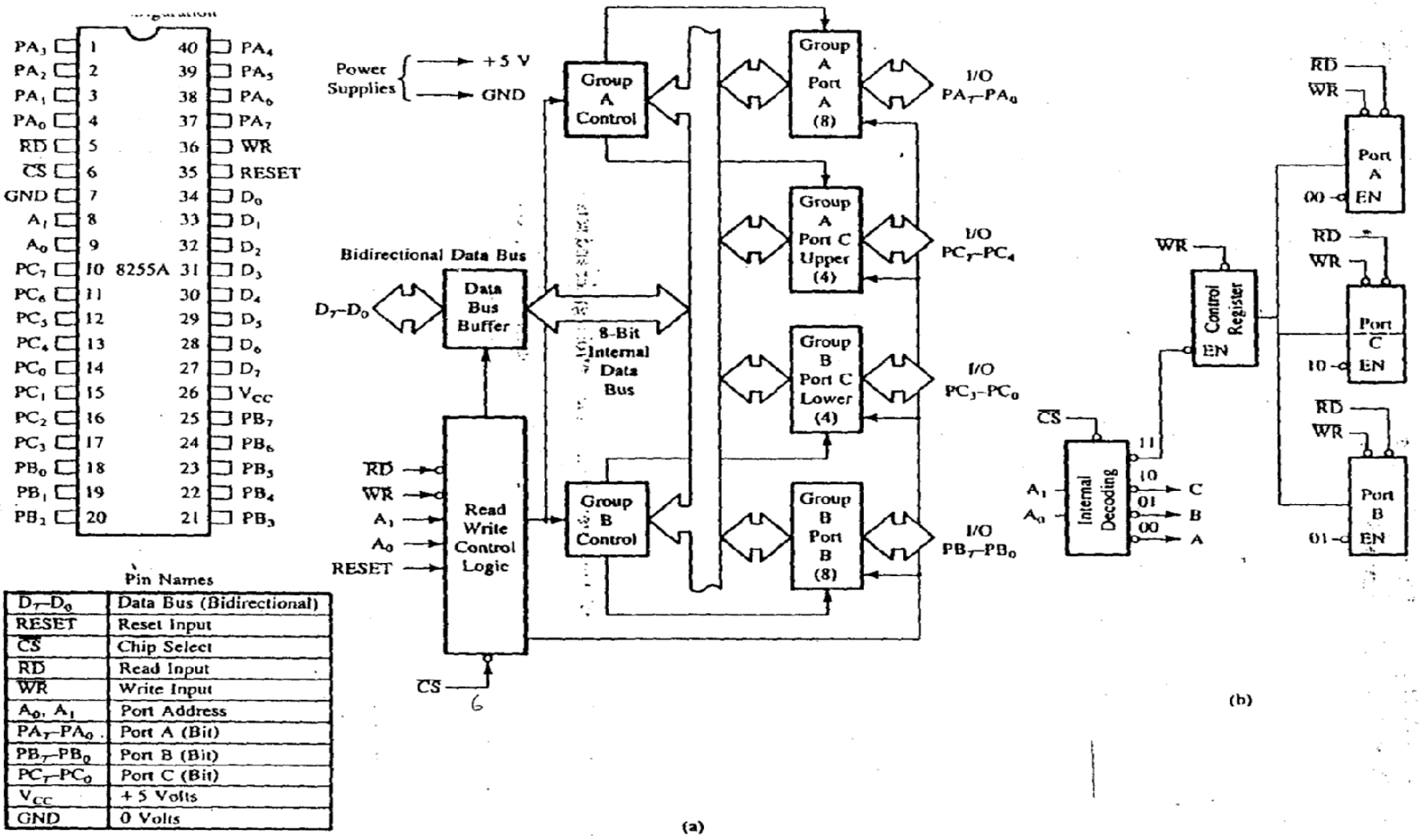
(b)

FIGURE 4.3

8255A Chip Select Logic (a) and I/O Port Addresses (b)

CONTROL WORD

Figure 4.2(b) shows a register called the control register. The contents of this register, called the control word, specify an I/O function for each port. This register can be accessed to write a control word when A0 and A1 are at logic 1, as mentioned previously. The register is not accessible for a Read operation.



Pin Names

D_7–D_0	Data Bus (Bidirectional)
RESET	Reset Input
$\overline{CS}$	Chip Select
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A_0, A_1	Port Address
PA_7–PA_0	Port A (Bit)
PB_7–PB_0	Port B (Bit)
PC_7–PC_0	Port C (Bit)
V_{CC}	+5 Volts
GND	0 Volts

FIGURE 4.2
8255A Block Diagram (a) and an Expanded Version of the Control logic and I/O Ports (b)

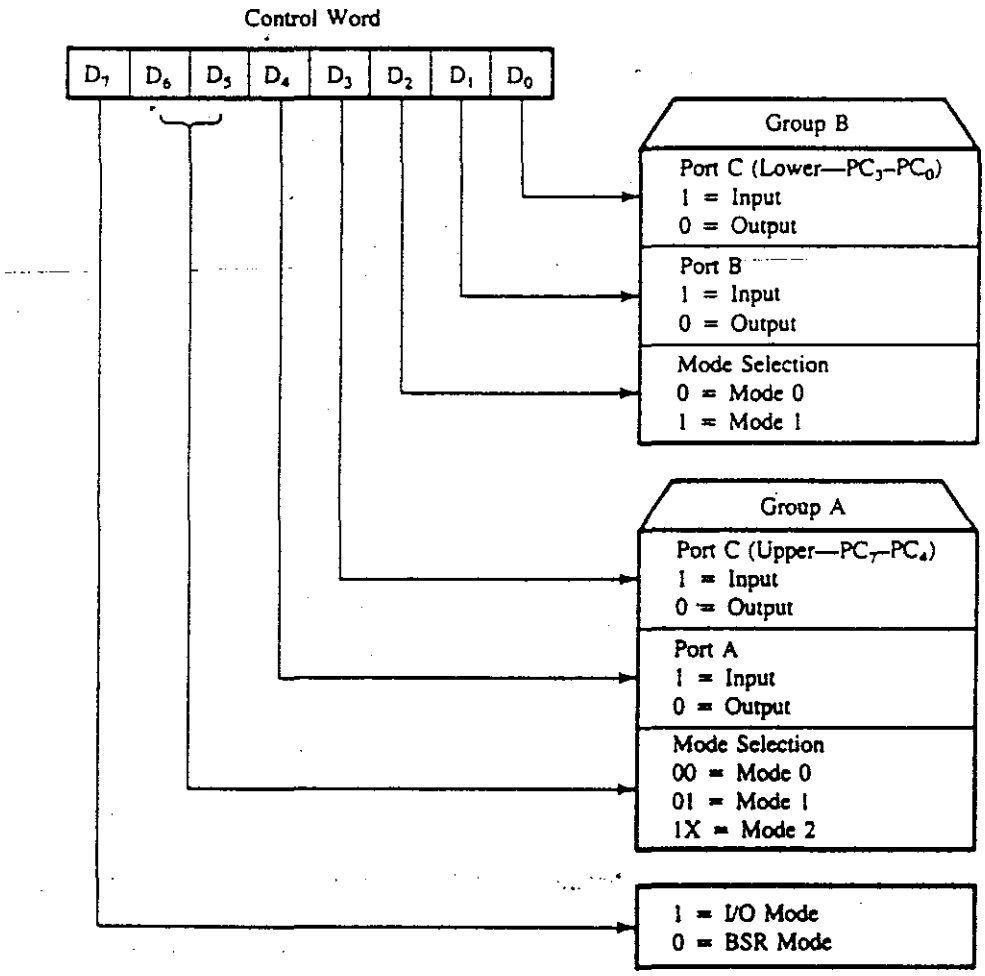


FIGURE 4.4

8255A Control Word Format for I/O Mode

Bit D7 of the control register specifies either the I/O function or the Bit Set/Reset function, as classified in Figure 4.1(b). If bit D7 = 1, bits D6—D0 determine I/O functions in various modes, as shown in Figure 4.4. If bit D7 = 0, port C operates in the Bit Set/Reset (BSR) mode. The BSR control word does not affect the functions of ports A and B (the BSR mode will be described later).

To communicate with peripherals through the 8255A, three steps are necessary:

1. Determine the addresses of ports A. B, and C and of the control register according to the Chip Select logic and address lines A0 and A1.
2. Write a control word in the control register.
3. Write I/O instructions to communicate with peripherals through ports A, B, and C.

Examples of the various modes are given in the next section.

4.1.2 Mode-0: Simple Input or Output

In this mode, ports A and B are used as two simple 8-bit I/O ports and port C as two 4-bit ports. Each port (or half-port, in case of C) can be programmed to function as simply an input port or an output port. The input/output features in Mode 0 are as follows:

1. Outputs are latched.
2. Inputs are not latched.
3. Ports do not have handshake or interrupt capability.

Example 4.1

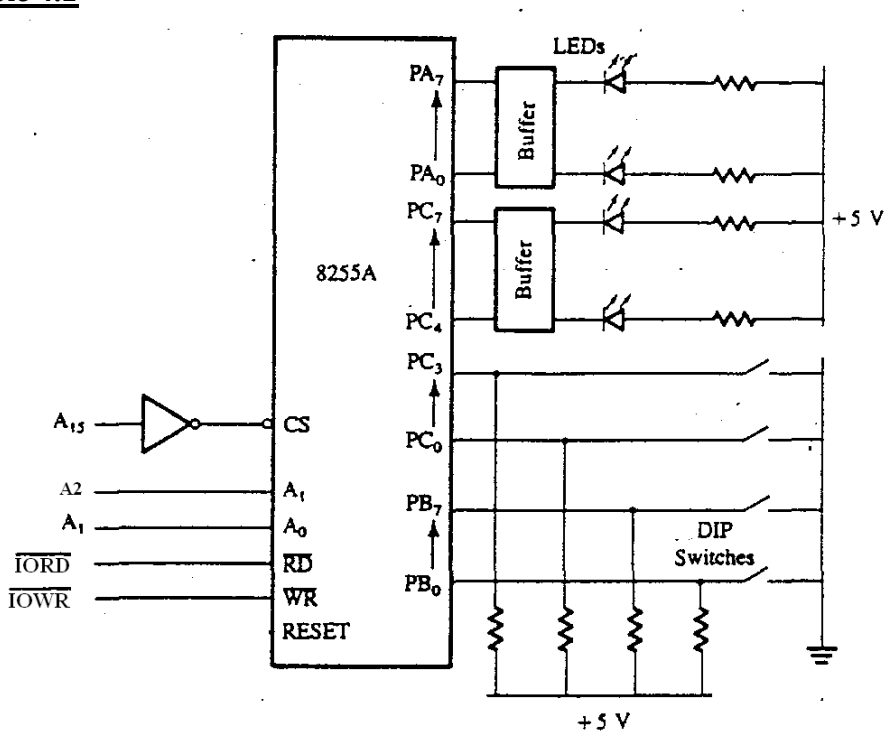


FIGURE 4.5

Interfacing 8255A I/O Ports in Mode 0

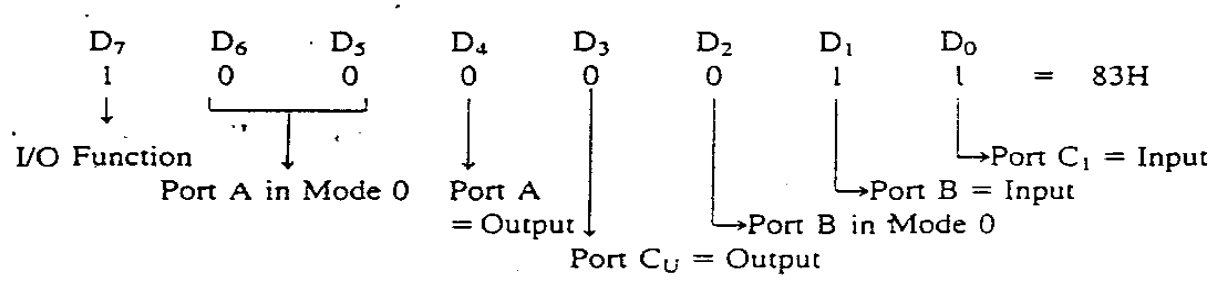
1. Identify the port addresses hi Figure 15.5.
2. Identify the Mode 0 control word to configure port A and port Cu as output ports and port B and port C_L as input ports.
3. Write a program to read the DIP switches and display the reading from port B at port A and from port CL at port Cu.

Solution

1. Port Addresses This is a standard I/O; when the address line A15 is high, the Chip Select line is enabled. Assuming all don't care lines are at logic 0, the port addresses are as follows:

Port A	=	8000H (A1 = 0, A2=0)
Port B	=	8002M (A1= l, A2 =0)
PortC	=	8004H (A1 = 0, A2 = 1)
Control Register	=	8006H (A1 = 1, A2 = 1)

2. Control Word



3. Program

```
CNWRD   EQ      83H
PORTA   EQ      8000H
PORTB   EQ      8002H
PORTC   EQ      8004H
CNREG   EQ      8006H

        MOV     AL, CNWRD   ;Load accumulator with the control word
        MOV     DX, CNREG   ;Control register address at DX
        OUT     DX, AL      ;Write word in the control register to initialize
                            ; the ports
        MOV     DX, PORTB   ; Port B address at DX
        IN      AL, DX      ;Read switches at port B
        MOV     DX, PORTA   ; Port A address at DX
        OUT     DX, AL      ;Display the reading at port A
        MOV     DX, PORTC   ; Port C address at DX
        IN      AL, DX      ;Read switches at port C
        ROL     AL, 4       ;Rotate and place data in the upper half of the
                            ;accumulator
        OUT     DX, AL      ;Display data at port CU
        HLT                 ;stop
```

Program Description The ports are initialized by placing the control word 83H in the control register. In this example, the low four bits of port C are configured as input and the high four bits are configured as output; even though port C has one address for both halves C, and C_L (8004H). When the MPU reads port C, it receives eight bits in the accumulator. However, the high-order bits (D7—D4) must be ignored because the input data bits are in PC3—PC0. To display these bits at the upper half of port C, bits (PC3—PC0) must be shifted to PC7—PC4.

4.1.3 BSR (Bit Set/Reset) Mode

The BSR mode is concerned only with the eight bits of port C, which can be set or reset by writing an appropriate control word in the control register. A control word with bit D7 = 0 is recognized as a BSR control word, and it does not alter any previously transmitted control word with bit D7 = 1; thus the I/O operations of ports A and B are not affected by a BSR control word. In the BSR mode, individual bits of port C can be used for applications such as an on/off switch.

BSR CONTROL WORD

This control word, when written in the control register, sets or resets one bit at a time, as specified in Figure 4.6.

Example 15.2

Write a BSR control word subroutine to set bits PC7 and PC3 and reset them after 10 ms. Use the schematic in Figure 4.3 and assume that a delay subroutine is available.

Solution BSR CONTROL WORDS

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
To set bit PC_7 =	0	0	0	0	1	1	1	1	= 0FH
To reset bit PC_7 =	0	0	0	0	1	1	1	0	= 0EH
To set bit PC_3 =	0	0	0	0	0	1	1	1	= 07H
To reset bit PC_3 =	0	0	0	0	0	1	1	0	= 06H

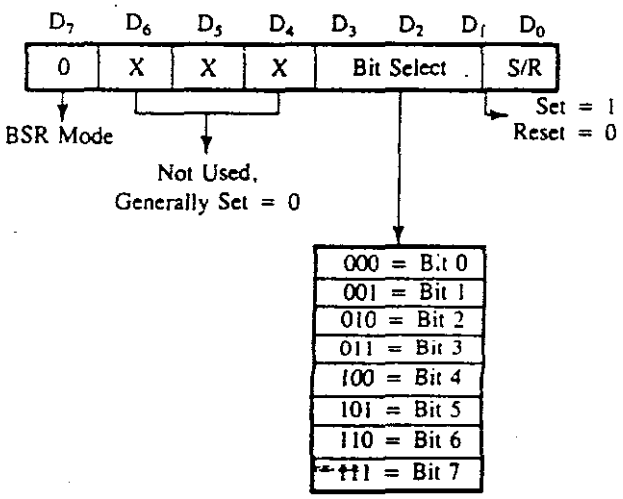


FIGURE 4.6 8255A Control Word Format in the BSR Mode

PORT ADDRESS
Control register address = 86H; refer to Figure 4.3(b).

SUBROUTINE

```
CNWRD   EQ    83H
STPC7   EQ    0FH
CLPC7   EQ    0EH
STPC3   EQ    07H
CLPC3   EQ    06H
CNREG   EQ    8006H

BSR:    MOV   DX, CNREG    ;Control register address at DX
        MOV   AL, STPC7    ;word to set PC7 in AL
        OUT   DX, AL       ;set PC7
        MOV   AL, STPC3    ;word to set PC3 in AL
        OUT   DX, AL       ;set PC3
        CALL  DELAY        ; This is a 10-ms delay
        MOV   AL, CLPC7    ;word to reset PC7 in AL
        OUT   DX, AL       ;reset PC7
        MOV   AL, STPC3    ;word to reset PC3 in AL
        OUT   DX, AL       ;reset PC3
        RET
        OUT   DX, AL       ;reset PC3
                           ;stop
```

From an analysis of the above routine, the following points can be noted:
1. To set/reset bits in port C, a control word is written in the control register and not in port C
2: A BSR control word affects only one bit in port C.
3. The BSR control word does not affect the I/O mode.

4.1.4 Illustration: Interfacing A/D Converter Using the 8255A in Mode 0 and BSR Mode.

PROBLEM STATEMENT

Design an interfacing circuit to read data from an A/D convener.

1. Set up port A to read data.
2. Set up bit PC0 to start conversion and bit PC7 to read the ready status of the convener.

PROBLEM ANALYSIS

The Chip Select logic in Figure 4.7 is the same as in Figure 4.5; therefore, the assigned port addresses range from 8000H for port A to 8006H for the control register.

MODE 0: CONTROL WORD

The configuration of the ports is specified follows:

Port A: As an input port.

Port CL: As an output port because bit PC0 is used to start conversion.

Port CU: As an input port to read the status at PC7.

Port B: not used.

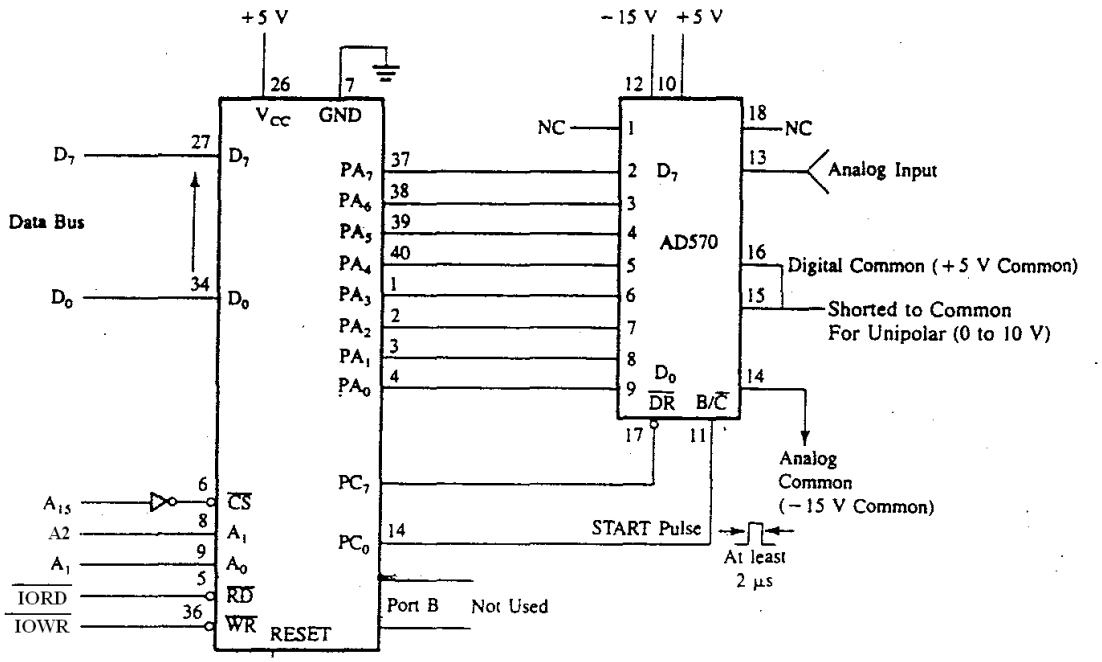
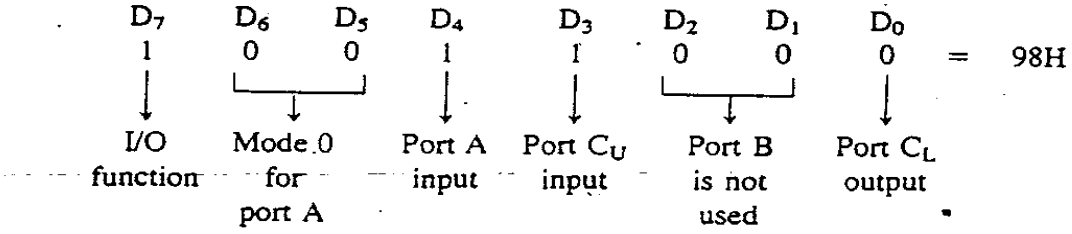


FIGURE 4.7

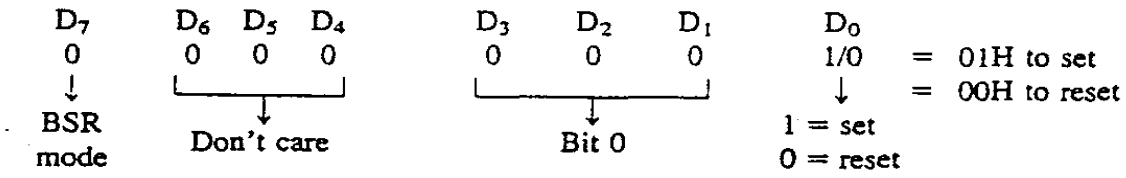
Schematic: Interfacing the A/D Converter AD570 Using the 8255A in Mode 0 and BSR Mode

Therefore, the control word necessary to meet the requirements is as follows:



BSR CONTROL WORD FOR START PULSE

Bit PC_0 is used as a START pulse. To set and reset PC_0, the BSR control word is as follows (refer to Figure 15.6):



SUBROUTINE

```
CNWRD   EQ    98H
STPC0   EQ    01H
CLPC0   EQ    00H
PORTA   EQ    8000H
PORTC   EQ    8004H
CNREG   EQ    8006H

A2D:    MOV   DX, CNREG     ;Control register address at DX
        MOV   AL, CNWRD     ;control word in AL
        OUT   DX, AL        ;Write word in the control register to initialize
                            ; the ports
        MOV   AL, STPC0     ;Load BSR control word to set PC0
        OUT   DX, AL        ;Turn on the START pulse
        CALL  DELAY         ; Wait
        MOV   AL, CLPC0     ; Load BSR control word to reset PC0
        OUT   DX, AL         ;Start conversion
        MOV   AL, STPC3     ;word to reset PC3 in AL
        OUT   DX, AL        ;reset PC3
        MOV   DX, PORTC
READ:   IN    AL, DX
        ROL   AL, 1
        JC    READ
        MOV   DX, PORTA
        IN    AL, DX
        RET
```

15.15 Mode 1: Input or Output with Handshake

In Mode 1, handshake signals are exchanged between the MPU and peripherals prior to data transfer. The features of this mode include the following:

1. Two ports (A and B) function as 8-bit I/O ports. They can be configured either as input or output ports.
2. Each port uses three lines from port C as handshake signals. The remaining two lines of port C can be used for simple I/O functions.
3. Input and output data are latched.
4. Interrupt logic is supported.

In the 8255A, the specific lines from port C used for handshake signals vary according to the I/O function of a port. Therefore, input and output functions in Mode 1 are discussed separately.

MODE 1: INPUT CONTROL SIGNALS

Figure 15.8(a) shows the associated control signals used for handshaking when ports A and B are configured as input ports. Port A uses the upper three signals: PC_3, PC_4, and PC_5. Port B uses the lower three signals: PC_2, PC_1, and PC_0. The functions of these signals are as follows:

- **$\overline{STB}$ (Strobe Input):** This signal (active low) is generated by a peripheral device to indicate that it has transmitted a byte of data. The 8255A, in response to $\overline{STB}$, generates IBF and INTR, as shown in Figure 15.9.

- **IBF (Input Buffer Full):** This signal is an acknowledgment by the 8255A to indicate that the input latch has received the data byte. This is reset when the MPU reads the data

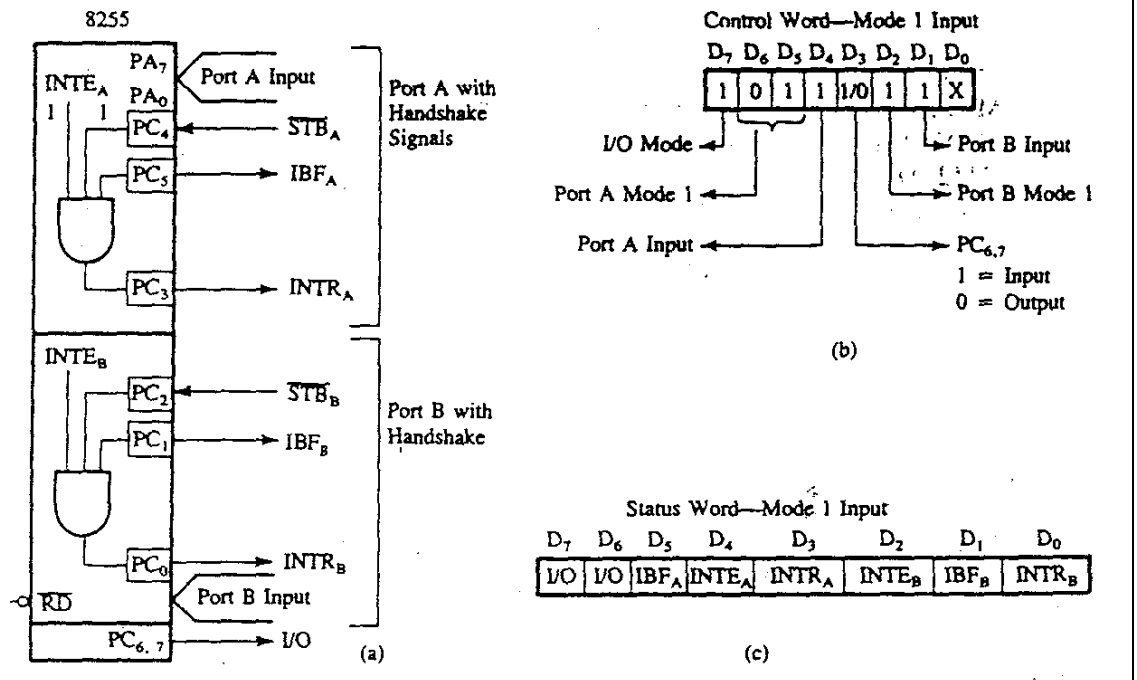


FIGURE 4.8

8255A Mode 1: Input Configuration

- **INTR (Interrupt Request):** This is an output signal that may be used to interrupt the MPU. This signal is generated if $\overline{STB}$, IBF, and INTE (Internal flip-flop) are all at logic 1. This is reset by the falling edge of the $\overline{RD}$ signal (Figure 4.9).
- **INTE (Interrupt Enable):** This is an internal flip-flop used to enable or disable the generation of the INTR signal. The two flip-flops $INTE_A$ and $INTE_B$ are set/reset using the BSR mode. The $INTE_A$ is enabled or disabled through PC_4, and $INTE_B$ is enabled or disabled through PC_2.

CONTROL AND STATUS WORDS

Figure 4.8(b) uses control words derived from Figure 4.4 to set up port A and port B as input ports in Mode 1. Similarly, Figure 4.8(c) also shows the status word, which will be placed in the accumulator if port C is read.

PROGRAMMING THE 8255A IN MODE 1

The 8255A can be programmed to function using either status check I/O or interrupt I/O. Figure 4.10(a) shows a flowchart for the status check I/O. In this flowchart, the MPU continues to check data status through the IBF line until it goes high. This is a simplified flowchart and does not show how to handle data transfer if two ports are being used. The technique is similar to that of Mode 0 combined with the BSR mode. The disadvantage of the status check I/O with handshake is that the MPU is tied up in the loop.

The flowchart in Figure 4.10(b) shows the steps required for the interrupt I/O, assuming that vectored interrupts are available. The confusing step in the interrupt I/O is to set INTE either for port A or port B. Figure 4.8(a) shows that the $\overline{STB}$ signal is connected to pin PC_4 and the $INTE_A$ is also controlled by the pin PC_4. (In port B, pin PC_2 is used for the same purposes.) However, the $INTE_A$ is set or reset in the BSR mode and the BSR control word has no effect when ports A and B are set in Mode 1.

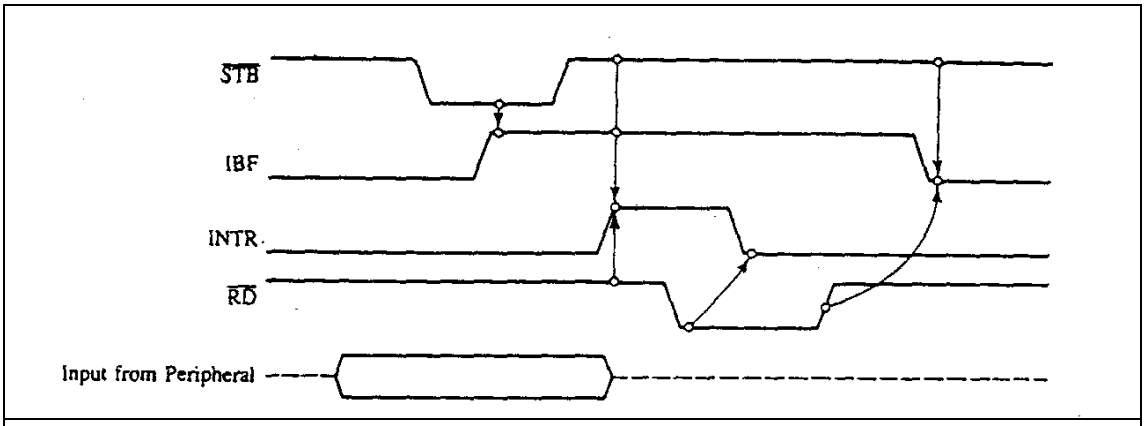


FIGURE 4.9
8255A Mode 1: Timing Waveforms for Strobed Input (with Handshake)

In case the INTR line is used to implement the interrupt, it may be necessary to read the status of $INTR_A$ and $INTR_B$ to identify the port requesting an interrupt service and to determine the priority through software, if necessary.

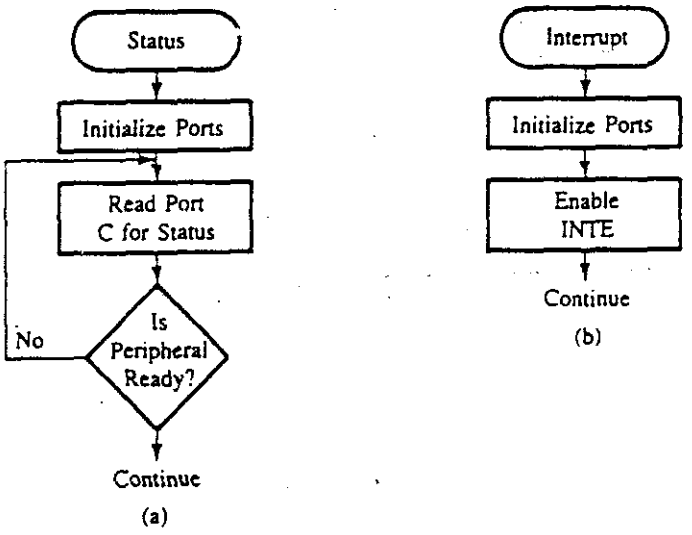


FIGURE 4.10
flowcharts: Status Check I/O (a) and Interrupt I/O (b)

MODE 1: OUTPUT CONTROL SIGNALS

Figure 4.11 shows the control signals when ports A and B are configured as output ports. These signals are defined as follows:

- **$\overline{\text{OBF}}$ (Output Buffer Full):** This is an output signal that goes low when the MPU writes data into the output latch of the 8255A. This signal indicates to an output peripheral that new data are ready to be read (Figure 4.12). It goes high again after the 8255A receives an $\overline{\text{ACK}}$ from the peripheral.
- **$\overline{\text{ACK}}$ (Acknowledge):** This is an input signal from a peripheral that must output a low when the peripheral receives the data from the 8255A ports (Figure 4.12).
- **INTR (Interrupt Request):** This is an output signal, and it is set by the rising edge of the $\overline{\text{ACK}}$ signal. This signal can be used to interrupt the MPU to request the next data byte for output. The INTR is set when $\overline{\text{OBF}}$, $\overline{\text{ACK}}$, and INTE are all one (Figure 4.12) and reset by the falling edge of $\overline{\text{WR}}$.
- **INTE (Interrupt Enable):** This is an internal flip-flop to a port and needs to be set to generate the INTR signal. The two flip-flops INTE_A and INTE_B are controlled by bits PC_6 and PC_2, respectively, through the BSR mode.
- **$\text{PC}_{4,5}$:** These two lines can be set up either as input or output.

CONTROL AND STATUS WORDS

Figure 4.11(b) shows the control word used to set up ports A and B as output ports in Mode 1. Similarly, Figure 4.11(c) also shows the status word, which will be placed in the accumulator if port C is read.

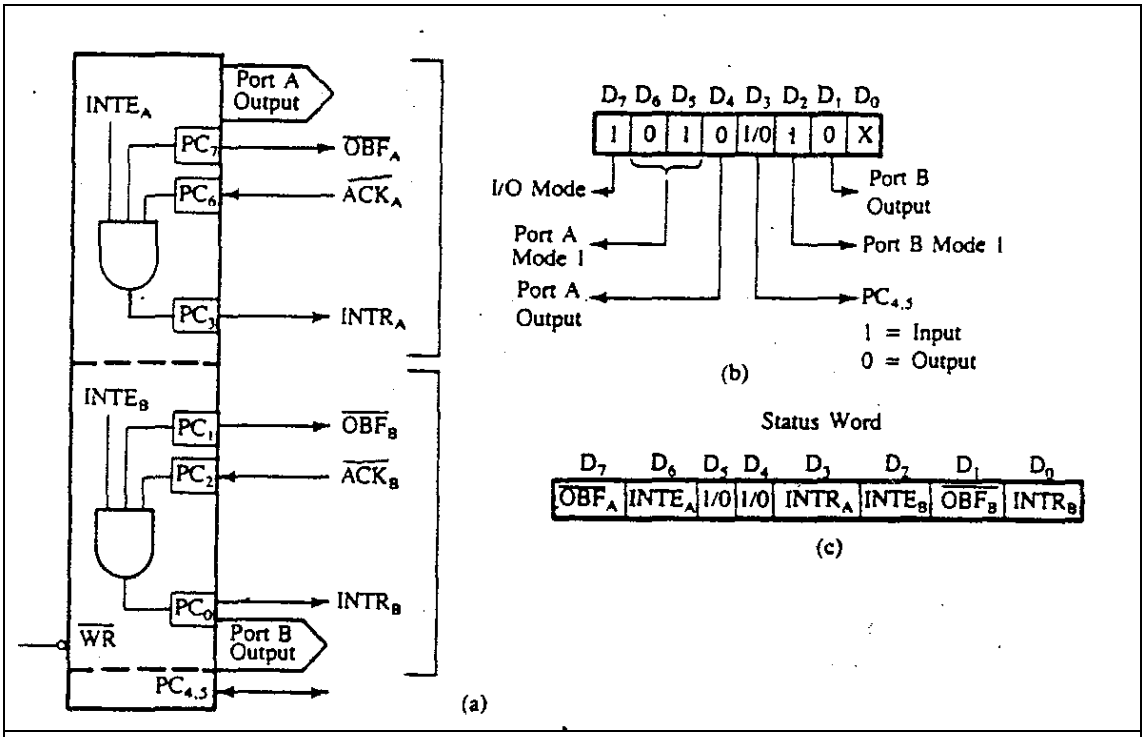


FIGURE 4.11
8255A Mode 1: Output Configuration

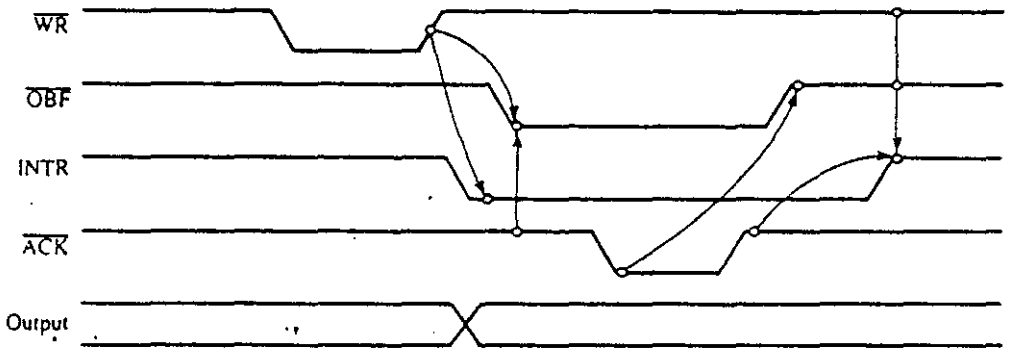


FIGURE 15.12
8255 Mode 1: Timing Waveforms for Strobed (with Handshake) Output

Illustration: An Application of the 8255A in the Handshake Mode (Mode 1)

PROBLEM STATEMENT

Figure 4.13 shows an interfacing circuit using the 8255A in Mode 1. Port A is designed as the input port for a keyboard with interrupt I/O, and port B is designed as the output port for a printer with status check I/O.

1. Find port addresses by analyzing the decode logic.
2. Determine the control word to set up port A as input and port B as output in Mode 1.
3. Determine the BSR word to enable $INTE_A$ (port A).
4. Determine the masking byte to verify the $\overline{OBF}_B$ line in the status check I/O (port B).
5. Write initialization instructions and a printer subroutine to output characters that are stored in memory.

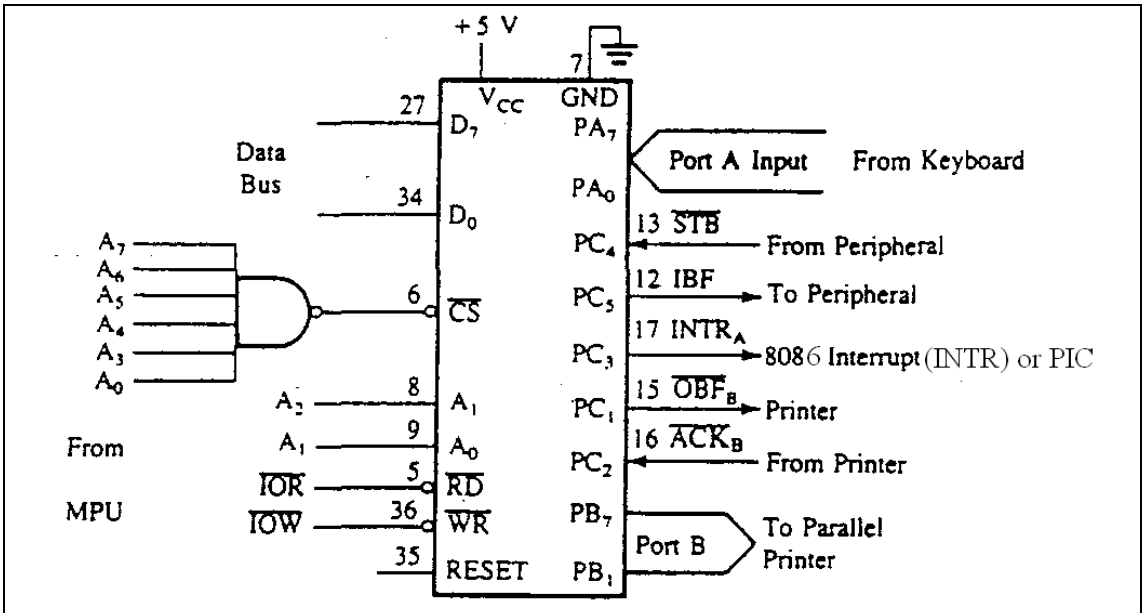


FIGURE 4.13
Interfacing the 8255A in Mode I (Strobed Input/Output)

1. Port Addresses The 8255A is connected as peripheral I/O. When the address lines A_7–A_0 are all 1, the output of the NAND gate goes low and selects the 8255A. The individual ports are selected as follows:

Port A = F8H ($A_2 = 0$, $A_1 = 0$)
Port B = FAH ($A_2 = 0$, $A_1 = 1$)
Port C = FCH ($A_2 = 1$, $A_1 = 0$)
Control Register = FEH ($A_2 = 1$, $A_1 = 1$)

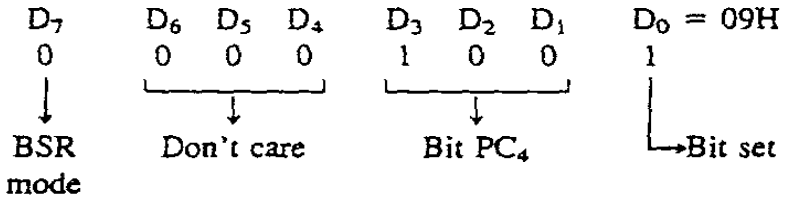
2. Control Word to Set Up Port A as Input and Port B as Output in Mode 1

D_7	D_6 D_5	D_4	D_3	D_2	D_1	D_0 = B4H
1	0 1	1	0	1	0	0
I/O function	Port A in Mode 1	Port A as input	$PC_{6,7}$ as don't care	Port B in Mode 1	Port B as output	Bit D_0 is don't care

In the above control word, all bits are self explanatory, and bits D_3 and D_0 are in a don't care logic state. To generate interrupt signal $INTR_A$, flip-flop $INTE_A$ should be set to 1, which can be accomplished by using the BSR Mode to set PC_4.

The output to the printer (port B) is status-controlled. Therefore, the status of line $\overline{OBF_B}$ can be checked by reading bit D_1 of port C_L.

3. BSR Word to Set $INTE_A$ To set the Interrupt Enable flip-flop of port A ($INTE_A$), bit PC_4 should be 1.



4. Status Word to Check $\overline{OBF_B}$

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
X	X	X	X	X	X	$\overline{OBF_B}$	X

Masking byte: 02H

5. Initialization Program

```
CNWRD   EQU   0B4H
CNREG   EQU   0FEH
STPC4   EQU   09H
MASK    EQU   02H
PORTA   EQU   0F8H
PORTB   EQU   0FAH
PORTC   EQU   0FCH
CNREG   EQU   0FEH

        MOV   AL, CNWRD  ;Word to initialize port A as input,
                         ;  port B as output in Mode 1
        OUT   CNREG, AL
        MOV   AL, STPC4  ;Set INTEA (PC4)
        OUT   CNREG, AL  ;Using BSR Mode
        STI              ;Enable interrupts
        CALL  PRINT
        ;Continue other tasks
```

Print Subroutine

```
MemPtr  EQU   2000H
COUNT   EQU   100

PRINT:  MOV   SI, MemPtr  ;Point index to location of stored characters
        MOV   CX, COUNT   ;Number of characters to be printed
NEXT:   MOV   AL, [SI]    ;Get character from memory
        MOV   BL, AL      ;Save character
STATUS: IN    AL, PORTC   ;Read port C for status of OBF
        AND   AL, MASK    ;Mask all bits except D1
```

```
JZ      STATUS      ;If it is low, the printer is not ready: wait in
                    ;a loop
MOV     AL, BL
OUT     PORTB, AL   ;Send a character to port B
INC     SI          ;Point to the next character
LOOP    NEXT        ; Repeat until count = 0
RET
```

PROGRAM DESCRIPTION

This I/O design using the 8255A in Mode 1 allows two operations: outputting to the printer and data entry through the keyboard. The printer interfacing is designed with the status check and the keyboard interfacing with the interrupt.

In the PRINT subroutine, the character is placed in the accumulator, and the status is read by the instruction IN FEH. Initially, port B is empty, bit PC_1 ($\overline{OBF_B}$) is high, and the instruction OUT FDH sends the first character to port B. The rising edge of the $\overline{WR}$ signal sets signal $\overline{OBF}$ low, indicating the presence of a data byte in port B, which is sent out to the printer (Figure 4.12). After receiving a character, the printer sends back an acknowledge signal ($\overline{ACK}$), which in turn sets $\overline{OBF_B}$ high, indicating that port B is ready for the next character, and the PRINT subroutine continues.

If a key is pressed during the PRINT, a data byte is transmitted to port A and the $\overline{STB_A}$ goes low, which sets IBF_A high. The initialization routine should set the $INTE_A$ flip-flop. When the $\overline{STB_A}$ goes high, all the conditions (i.e., $IBF_A = 1$, $INTE_A = 1$) to generate $INTR_A$ are met. This signal, which is connected to a PIC, which, interrupts the MPU, and the program control is transferred to the service routine. This service routine would read the contents of port A, enable the interrupts, and return to the PRINT routine (the interrupt service routine is not shown here).

4.17 Mode 2: Bidirectional Data Transfer

This mode is used primarily in applications such as data transfer between two computers or floppy disk controller interface. In this mode, port A can be configured as the bidirectional port and port B either in Mode 0 or Mode 1. Port A uses five signals from port C as handshake signals for data transfer. The remaining three signals from port C can be used either as simple I/O or as handshake for port B. Figure 4.14 shows two configurations of Mode 2.

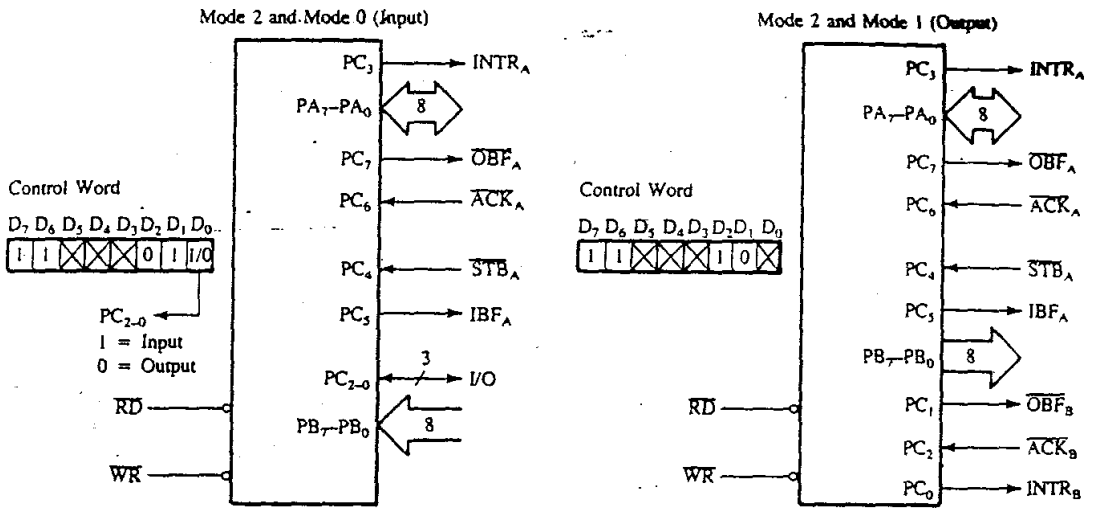


FIGURE 4.14

8255A Mode 2: Bidirectional Input/Output